

### AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions or listings of claims for this application.

#### Listing of Claims:

1. (Currently amended) A pixel cell comprising:  
a photo-conversion device that generates charge;  
a gate controlled charge storage region that stores the ~~photo-~~  
~~generated~~ charge under control of a control gate, and  
a first transistor having its gate between the photo-conversion device  
and the charge storage region for transferring ~~photo-generated~~ charge from the  
photo-conversion device to the charge storage region.
2. (Original) The pixel cell of claim 1, wherein the charge storage  
region is part of a buried channel MOS capacitor.
3. (Original) The pixel cell of claim 1, wherein the charge storage  
region is below a surface of the substrate.
4. (Original) The pixel cell of claim 1, wherein the charge storage  
region comprises:  
a doped region of a second conductivity type; and  
a doped surface layer of a first conductivity type over and in contact  
with the doped region of a second conductivity type, the control gate being  
over the doped surface layer.
5. (Original) The pixel cell of claim 1, wherein the control gate  
comprises polysilicon doped with a first conductivity type dopant.

6. (Original) The pixel cell of claim 1, wherein the first transistor is a shutter transistor for determining an integration time for the pixel cell.

7. (Currently amended) ~~The pixel cell of claim 1, further comprising: A~~  
pixel cell comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the charge under control of a control gate,

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring charge from the photo-conversion device to the charge storage region;

a sensing node; and

a second transistor having its gate between the charge storage region and the sensing node.

8. (Original) The pixel cell of claim 7, wherein the sensing node is a floating diffusion region.

9. (Original) The pixel cell of claim 7, wherein the control gate at least partially overlaps the first and second transistor gates.

10. (Original) The pixel cell of claim 1, wherein the photo-conversion device is a pinned photodiode.

11. (Currently amended) A pixel cell comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the ~~photo-generated~~ charge under control of a control gate, wherein the charge storage region comprises a doped region of a second conductivity type and a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, and wherein the control gate is over the doped surface layer; and

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring ~~photo-generated~~ charge from the photo-conversion device to the charge storage region.

12. (Original) The pixel cell of claim 11, wherein the charge storage region is part of a buried channel metal oxide semiconductor (MOS) capacitor.

13. (Currently amended) ~~The pixel cell of claim 11, further comprising:~~  
A pixel cell comprising:

a photo-conversion device that generates charge;

a gate controlled charge storage region that stores the charge under control of a control gate, wherein the charge storage region comprises a doped region of a second conductivity type and a doped surface layer of a first conductivity type over and in contact with the doped region of a second conductivity type, and wherein the control gate is over the doped surface layer;

a first transistor having its gate between the photo-conversion device and the charge storage region for transferring charge from the photo-conversion device to the charge storage region;

a sensing node; and  
a second transistor having its gate between the charge storage region  
and the sensing node.

14. (Original) The pixel cell of claim 13, wherein the control gate  
overlaps the first and second transistor gates.

Claims 15-45 (Canceled).